List of effective pages for:

CU SERVICE MANUAL

(Preliminary Version)

for

P850 - P855 - P860

Date of printing 1st March 1972

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SECTION V

DIGITAL INPUT/OUTPUT SYSTEM (DIOS)

BRIEF DESCRIPTION

The Digital Input/output system provides the interface and control logic required to transfer information between digital peripheral equipment and the programmed channel of an 800 Series computer. The DIOS may be supplied in any of the following forms to suit the requirements of the customer:

(i) Digital Input Controller (DIC): to provide the interface buffering and control logic for four 16-bit input channels (A, B, C and D) see block diagram Figure 5.4. The DIC is contained on one card.

(ii) Digital Output Controller (DOC): to provide the interface buffering and control logic for four 16-bit output channels, see block diagram Figure 5.5. The DOC is contained on one card.

(iii) Digital Input/Output Controller (DIOC) to provide the interface and control logic for two input (A and B) and two output (C and D) 16-bit channels, see block diagram Figure 5.6. The DIOC is contained on one card.

In addition to the basic cards described above optional cards may be used to provide:

(a) Buffering of the incoming data - there are no storage facilities in either the DIC or DIOC for incoming lines.

(b) Change of state detection - to inform the computer when a change of data on the incoming data lines occurs.

(c) Level adaptation - to match the interface logic levels with those of the digital equipment.

(d) Galvanic isolation and level adaptation - to completely isolate, electrically, the external digital equipment from the system.

5.1 ADDRESSING

The address of the DIOS may be selected using straps which connect the address decode gate (shown on the schematic diagram) in the DIOS to BAD lines 00-03. The address part of instructions are checked when a

validity signal DAV is received from the computer. If the address is accepted the signal $\overline{ARE}$ is returned to the computer and function decoding is enabled. If a data transfer function is requested the channel address is specified on BAD lines 04 and 05 as follows and decoded by the Channel Select gates once the controller address has been accepted.

BAD 04	05	
0	0	Channel A
0	1	Channel B
1	0	Channel C
1	1	Channel D

5.2 FUNCTION DECODING

The function of instruction is determined by BOF lines 00-02. The functions recognized by each of the DIOS units are as follows:

BOF Lines 00	01	02	Function	Recognized by
1	0	1	Input Channel Address (INR)	All units
1	0	0	Input Data Word (INR)	DIC and DIOC
0	0	0	Output Data Word (OTR)	DOC and DIOC

When a function code is accepted the signal ACC is returned to the computer.

5.3 SEQUENCE OF OPERATION

The following description is applicable to all the DIOS units except where otherwise stated. Data transfer between the device and the computer may be initiated by either.

(i) Control from the device

Where the transfer is initiated by the device, a CAL signal must be generated and sent to the DIOS to request each 16-bit word transfer. The CAL signal is stored in the DIOS by the Call flip-flops, one for each channel, and an interrupt (IR) is sent to the computer. The computer responds to the interrupt with an Input Channel Address INR instruction. If this instruction is accepted the Interrupt flip-flop in the DIOS is reset and the Call and Output gates enabled to place the contents of the Call flip-flops on Input Lines BIN15-12. Output gates are not required in the DOC and the

CAL information is placed directly onto the input lines via the Call gates. The CAL information is examined in the computer to determine the channel address demanding the transfer and whether an input or output transfer is required; the latter is defined by the type of unit or in the case of the DIOC the channel address (A and B are input channels and C and D are output channels). A second instruction is then sent to the DIOS to enable the data transfer.

(ii) Input:

For incoming transfers an Input Data Word INR instruction is sent to the DIC or DIOC with the DIOS address and channel number specified as described previously. If the instruction is accepted the Output gates and Channel Select gates are enabled. The output from the Channel Select gate returns a response signal (AOK, BOK, COK or DOK) to the channel which initiated the transfer, resets the Call flip-flop for that channel and enables the appropriate Input gates to transfer the information onto the BIN lines. The response signals to the device, may be delayed between 2 and 20 μs, see paragraph 5.7

(iii) Output:

For output data transfers an Output Data Word (OTR) is sent to the DOC or DIOC with the address and channel number specified as described previously. The instruction is handled in much the same way as the INR described above but with the information on the computer output lines (BOU) being clocked into the appropriate Channel Buffer instead of the Input gates being enabled.

(iv) Software Control:

Data may be transferred to and from a digital device under software control without a CAL signal from the device. Input Data Word instructions are used to sample the input lines from the device at intervals controlled by the software, see INPUT above. Output data is loaded into the buffers in the DIOS by Output Data Word OTR instructions. A response signal (AOK, BOK, COK, or DOK) is sent to the device when the buffer is loaded. The data will remain in the Output buffer until over written by new data from the computer.

5.4 TIMING

The timing of data transfers through the DIOS is solely dependant on the I/O bus timing see section 1 figure 1.2. Since no buffering is provided for the standard DIOS input channels, data could be lost if CAL interrupts are not serviced promptly.

5.5 RESETTING

The CALL flip-flops can be either reset together by a MC (Master Clear) signal from the computer or individually when the computer responds to the CAL. The INTERRUPT flip-flop is also reset by a MC signal or when the computer responds to the CAL.

5.6 DIOS to DEVICE INTERFACE

Connections between the DIOS and the digital devices are made using twisted pair wires between ELCO connectors. The DIOS interface in its standard form, without optional circuits, will match with normal TTL or DTL digital devices.

5.7 SPECIAL DELAY CIRCUIT

General:

The circuit is used to delay the DIOS response (OK) signals. The delay of the response signal can be adjusted, within the limits 1 μs, 20 μs, by changing the value of R1. Figure 5.7 is a schematic diagram of the delay circuit.

Circuit characteristics:

Input Low	0.2V - Fan In	2
Input High	0.4V - Fan In	2
Output Low	0.2V - Fan Out	10
Output High	3.2V - Fan Out	10.

Power is supplied from the processor - 5V ± 5%

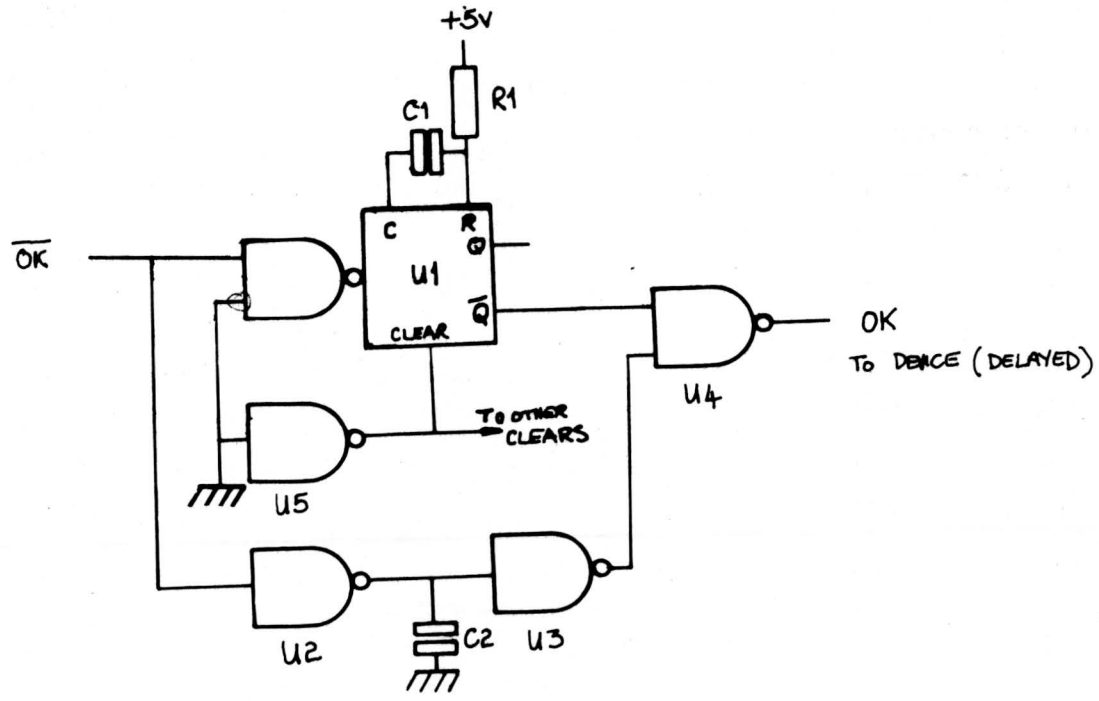
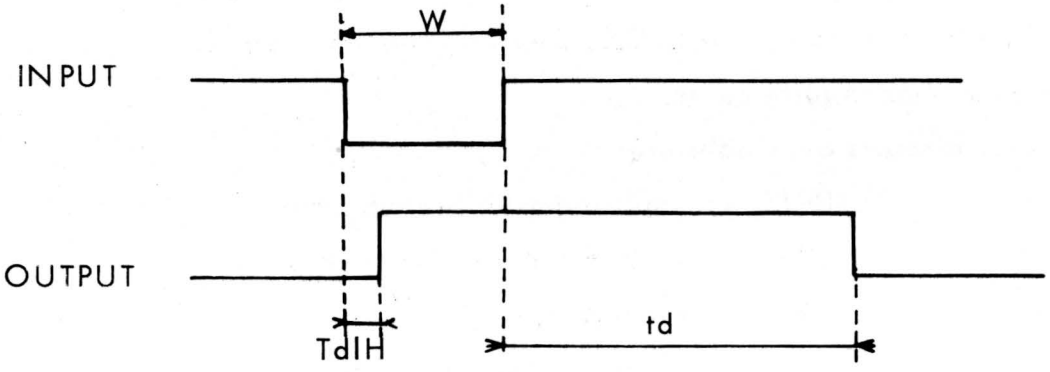


Figure 5.7 Schematic diagram of delay circuit



Timing measurements with the input driven by a TTL gate and the output open:

TdIH = 45nS typical

Td = 19.6μS typical

W = undefined

The delay provided by the circuit may be adjusted by changing resistor R1 as shown in the table below:

R1	Td
17.8K	19.6μS
8.25K	9.1μS
4.64K	5.1μS
2.61K	2.57μS
1.33K	1.46μS
825Ω	0.910μS

Components:

R1	1 X 17.8K	1/8W
C1	1 X 3.3nF	Ceramic plate
C2	1 X 330pF	Ceramic plate
U1	1/2 74123	
U2	1/6 7404	
U3	1/6 7404	
U4	1/4 7400	
U5	1/6 7404	

5.8 EXTENDED DIOS

Special circuits may be used to extend the facilities provided by the standard DIOS and adapt the DIOS/ Device interface to match specific customer requirements.

The special circuits available are:

INIS - Input adaptor Not ISolated

ONIS - Output adaptor Not ISolated

IIS - Input adaptor ISolated

OIS - Output adaptor ISolated

5.9 SPECIAL CIRCUIT CARD (INIS)

The INIS card may be used with either a DIC or DIOC to buffer and provide change of stage detection circuits for two 16-bit input channels. The INIS card also provides logic levels changers to match the control and data logic levels of the device to those of the DIOS. The INIS card may be supplied in either of two forms:

(i) The INIS LT, to match symetrical input logic levels to those of the DIOS (high input +6V low input -6V)

(ii) The INIS HT to match assymetric input logic levels to those of the DIOS (high input +15V, low input 0V).

The level changing is achieved by receiver circuits, one for each of the incoming lines. The receiver circuit characteristics are given below.
If any of these functions are not required they may be strapped out on the INIS card itself. Figure 5.8 shows a block diagram of the INIS and Figures 5.9 -5.12 show the circuits in detail.

RECEIVING CIRCUITS

For INIS LT -	High Input +6V	Output +0.2V	Threshold
	Low Input -6V	+4.7V	voltage 1.5V
For INIS HT -	High Input +12V	Output +0.2V	Threshold
	Low Input 0V	+4.7V	voltage 5.9V

The digital device is connected to the INIS receiver circuits according to the distance between them, in the following way:

Distance	Connection	Noise Margin	Input -	High	Low
< 15M	single wires	> 3V	INISLT	≥5V	≤ -2.2V
			INISHT	≥10.5V	≤ 1.5V
> 15M <50M	twisted wires	> 4V	INISLT	≥ 6V	≤ -3.2V
			INISHT	≥11.5V	≤ 0.5V
> 50M	twisted wires	> 6V			

DRIVER CIRCUITS

Driver circuits are used to amplify the output from the receiver circuits sufficiently to drive the D flip-flops and the change of state detection logic. The same driver circuits are used through out the INIS and have the following characteristics:

Low	Input	0.2V	Output 0.2V with ISINK = 50mA
High	Input	3.3V	Output 47V V sup = 48V I load = 0.1mA.

TRANSFER LOGIC

Data on the Input lines may be clocked into the D flip-flops by either a RESPONSE signal from the computer or a CALL signal from the device. If the digital device cannot supply CALL signals change of state detection logic in the INIS may be used in place of the CALL signal to clock information into the buffer. The change of state logic triggers a monostable when the data on the incoming lines changes, the 1μs ground pulse produced generates a CALL signal for the DIOS and clocks the data into the buffer.

TRANSMITTING CIRCUITS

The transmitting circuits are switching transistors used to relay the computer's RESPONSE signal to the device. The supply for the transistors is taken from the device itself and must be adjusted according to the transmitting distance as follows:

Distance	Type of Connection	Output High
< 15M	single wires	> 12V
> 15M	twisted wires	> 15V
> 50M	twsited wires	> 24V

COMPONENTS

R1 - R34	34 x	121 Ω	1/8 W
R35 - R68	34 x	46,4 KΩ	1/8 W
R69 - R102	34 x	10 KΩ	1/8 W
R103 - R136	34 x	4,64 KΩ	1/8 W
R137 - R168	32 x	10 KΩ	1/8 W
R169 - R170	2 x	681 Ω	1/8 W
R171 - R172	2 x	261 Ω	1/8 W
R173 - R174	2 x	21,5 KΩ	1/8 W
R175 - R176	2 x	17,8 KΩ	1/8 W
R177	1 x	215 KΩ	1/8 W
R178	1 x	1 KΩ	1/8 W
R179		12,1 Ω	1/8 W

TS1 - TS67	66 x	BSX 20	
TS67 - TS68	2 x	BUY 47	

C1 - C34	34 x	330 pF	Ceramic plate
C35 - C68	34 x	1,5 nF	Ceramic plate
C69 - C100	32 x	100 pF	Ceramic plate
C101 - C102	2 x	100 pF	Ceramic plate
C103 - C120	18 x	3,9 nF	Ceramic plate
C121 - C122	2 x	0,47µF	Moulded
C123	1 x	0,47µF	Moulded
C124	1 x	0,47µF	Moulded

5.10 SPECIAL CIRCUIT CARD (OIS)

The OIS card may be used to provide electrical isolation and interface circuits to connect between the two 16-bit output channels and the control signals of a DIOC or DOC and digital peripheral equipment.

ISOLATION

Complete electrical isolation is acheived using optically coupled isolators (TIL111). The input to the isolator drives a light emitting gallium arsenide diode. The light from the diode is detected by a photo sensitive transistor and then further amplified to match the output requirements of the circuit. The power required for the input and output parts of the isolators are supplied separately by the device and the DIOS. The voltages supplied by the device are regulated in the OIS card, one regulator for each channel (see figure 5.15).

INPUT SIGNALS

A CAL signal for each channel may be input to the DIOS via the OIS card; they are isolated as described above (see figure 5.14). A two wire cable must be used between the device and the input to the isolator. The length of the cable is not limited, provided the noise delivered at the card is less than 3V peak. The output to the DIOS, loaded by 1 TTL, is as follows:

Output Low +0.3V
Output High +4.7V.

OUTPUT SIGNALS

Two output data channels and the response signals for those channels may be transmitted via the OIS card (see figure 5.13). Since the output transistors of the isolator receive their power from the device, the output signal level may be changed, to suit the distance between the device and the card, by adjusting the supply voltage.

Distance	Type of Connection	Output High
$<$15M	Single wire	$>$ 12V
$>$15M $<$50M	Twisted wires	$>$ 15V
$>$ 50M	Twisted wires	$>$ 24V

COMPONENTS

R1 to R17 and R69 to R85	34	21,5 K	1/8 W	5122 000 01362
R18 to R34 and R86 to R102	34	825	1/8 W	05391
R35 to R51 and R103 to R119	34	2,15 K	1/8 W	05431
R52 to R68 and R120 to R136	34	261	1/8 W	00902
R137 and R138	2	3,16 K	3/4 W	03421
R139 and R140	2	3,83 K	1/8 W	01182
R141 and R142	2	3,16 K	1/8 W	01162
R143 and R146	2	8,25 K	1/4 W	04782
R144, R145 and R147 and R148	4	562	1/8 W	05382
TS1 to TS34	34	BUY 47	T05	
TS35 and TS36	2	BSX 20	T018	
TS37 and TS39	2	MJ 2253	T066 with 1 B66 B2B	
TS38 and TS40	2	2N2907A	T018	
Gr1 and Gr2	2	BZY 88	5,6 V	
u1 to u36	36	TIXL 111	(1/2 package dual inline 6 pins)	
C1	1	0,47 uF		2222 344 90022

5.11 SPECIAL CIRCUIT CARD (IIS)

The IIS card may be used to provide electrical isolation and interface circuits to connect between the two 16-bit input channels and the control signals of a DIOC or DIC and digital peripheral equipment.

ISOLATION

Complete electrical isolation is acheived using optically coupled isolators (TIL111). The input to the isolator drives a light emitting gallium arsenide diode. The light from the diode is detected by a photo sensitive transistor and then further amplified to match the output requirements of the circuit. The power required for the input and output parts of the isolators are supplied seperately by the device and the DIOS.

INPUT SIGNALS

Two input data channels and a CAL signal for each channel may be input to the DIOS via the IIS card. These are isolated as described above (see figure 5.17). A two wire cable must be used between the device and the input to the isolator; either twisted pair or coaxial. The length of the cable is not limited provided the noise delivered at the card is less than 3V peak. The output to the DIOS, loaded by one TTL, is as follows:

Output low + 0.3V
Output high + 4.7V.

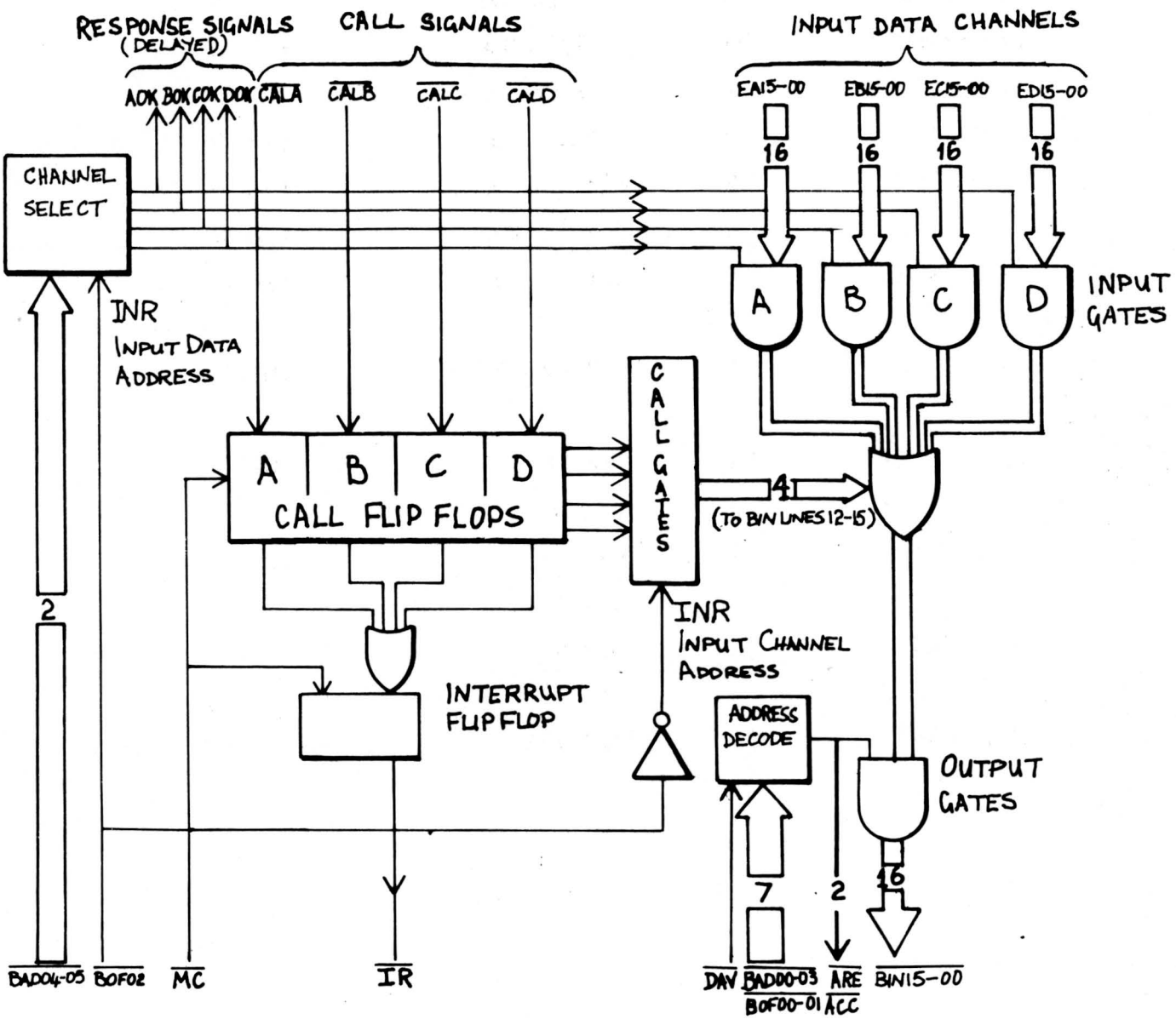
OUTPUT SIGNALS

A response signal for each of the input channels may be transmitted to the digital device via the IIS card. The response signals are isolated as described previously. The power for the output half of the isolators is supplied by the device and regulated in the IIS card (see figure 5.16). The output signal level can therefore be changed by adjusting the supply voltage to suit the distance between the device and the card.

COMPONENTS

R1 to R34	34	3,16 Kn	3/4 W
R35 to R68	34	3,83 Kn	1/8 W
R69 to R102	34	3,16 Kn	1/8 W
R103, 104	2	3,83 Kn	1/2 W
R105, 106	2	21,5 Kn	1/8 W
R107, 108	2	825 n	1/8 W
R109, 110	2	2,15 Kn	1/8 W
R111, 112	2	261 n	1/8 W
C1	1	0,47 µF	T018
TS1 to TS34	34	BSX 20	T018
TS35, 36	2	BUY 47	T05
TS37, 38	2	BUY 47	T05
Gr1, Gr2	2	BZY 88	11 V
u1 to u36	36	TIXL 111	(1/2 package dual in line).

DIGITAL EQUIPMENT



COMPUTER

ADDRESS LINES

BAD 00 01 02 03 04 05

DIC ADDRESS | CHANNEL NUMBER

FUNCTION LINES

BOF 00 01 02

1 0 0 INPUT DATA WORD

1 0 1 INPUT WORD ADDRESS

INPUT TO COMPUTER

BIN15-00 - DATA WORD

IR - INTERRUPT REQ

ARE - ADDRESS RECOGNISED

ACC - COMMAND ACCEPTED

OUTPUT FROM COMPUTER

MC - MASTER CLEAR

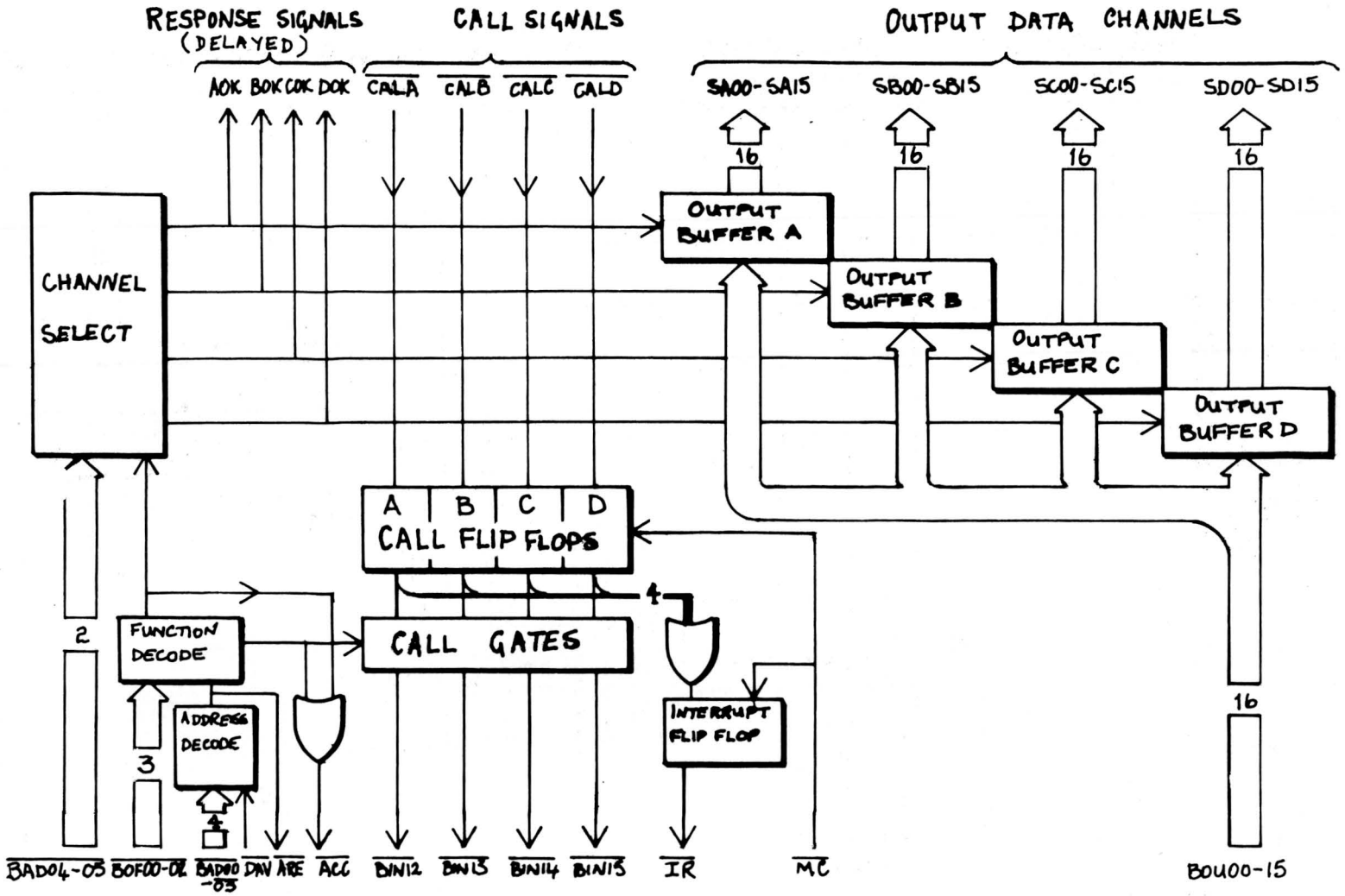
DAV - ADDRESS VALIDATOR

FUNCTION LINES

ADDRESS LINES

FIGURE 5.4 DIGITAL INPUT CONTROLLER

DIGITAL EQUIPMENT



COMPUTER

ADDRESS LINES

BAD 00 01 02 03 04 05

- 00 01 02 03 — DOC ADDRESS
- 04 05 — CHANNEL NUMBER

FUNCTION LINES

BOF000102

- 1 0 1 INPUT CHAN ADD
- 0 0 0 OUTPUT DATA WORD

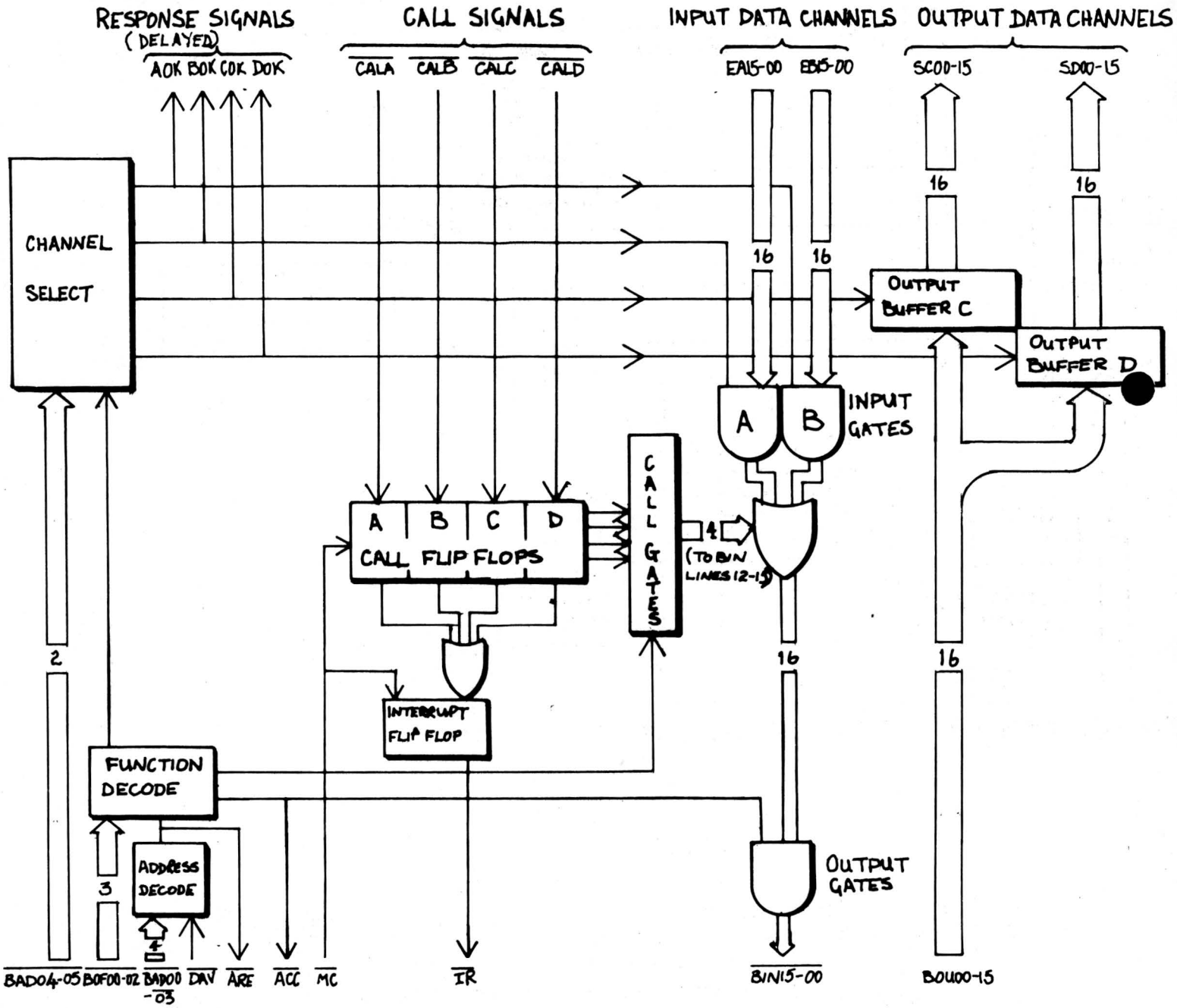
INPUT TO COMPUTER

- BIN12-15 — CALL WORD
- IR — INTERRUPT REQ
- ARE — ADDRESS RECOGNISED
- ACC — COMMAND ACCEPTED

OUTPUT FROM COMPUTER

- BOU00-15 — DATA WORD
- MC — MASTER CLEAR
- DAV — ADDRESS VALIDATOR
- FUNCTION LINES
- ADDRESS LINES

FIGURE 5.5 DIGITAL OUTPUT CONTROLLER



COMPUTER

ADDRESS LINES

BAD 00 01 02 03 04 05

- 00 01 02 03: DIOC ADDRESS
- 04 05: CHANNEL NUMBER

FUNCTION LINES

BOF 00 01 02

- 1 0 0 INPUT DATA WORD
- 1 0 1 INPUT CHANNEL ADD
- 0 0 0 OUTPUT DATA WORD

INPUT TO COMPUTER

- BIN15-00 - DATA WORD
- IR - INTERRUPT REQ
- ARE - ADDRESS RECOGNISED
- ACC - COMMAND ACCEPTED

OUTPUT FROM COMPUTER

- BOU00-15 - DATA WORD
- MC - MASTER CLEAR
- DAV - ADDRESS VALIDATOR
- FUNCTION LINES
- ADDRESS LINES

FIGURE 5.6 DIGITAL INPUT/OUTPUT CONTROLLER

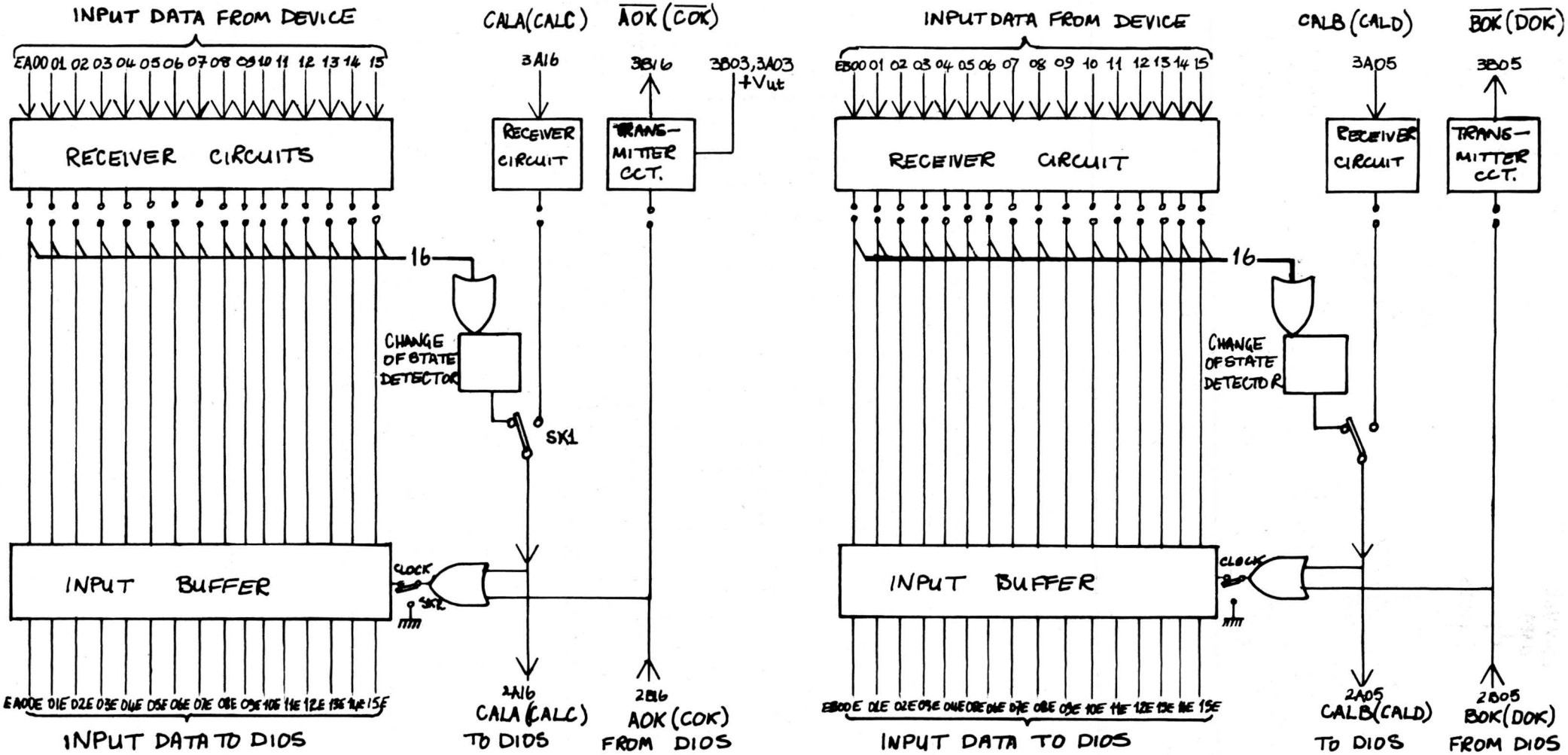


Fig 5.8 SPECIAL CIRCUIT CARD INIS

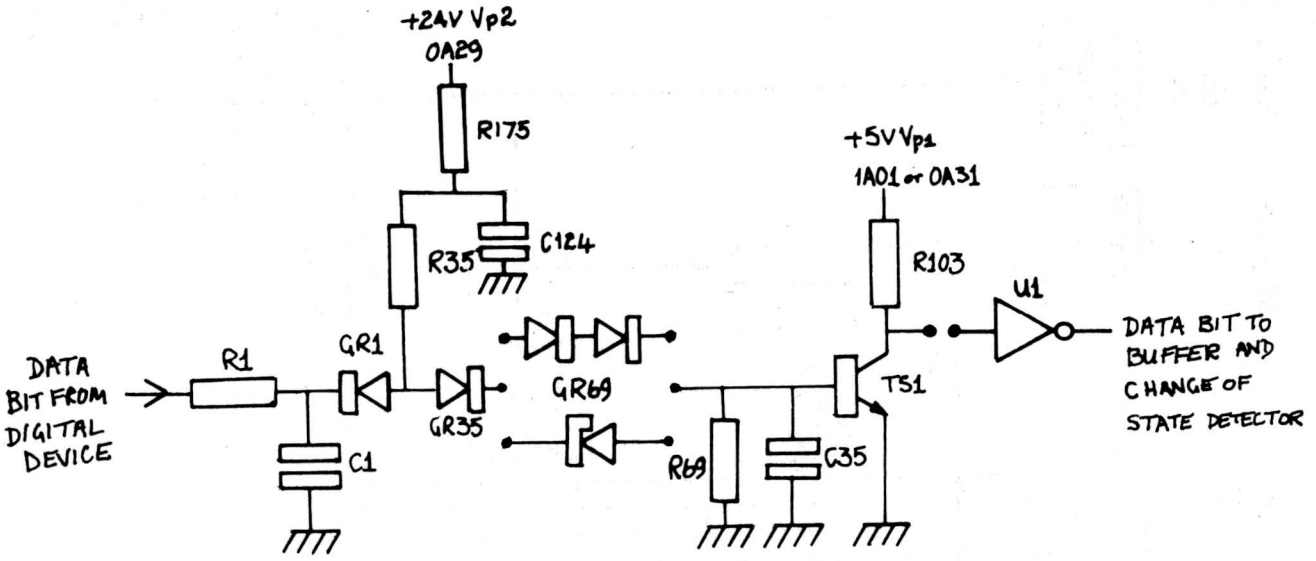


FIGURE 5.9 RECEIVER CIRCUIT

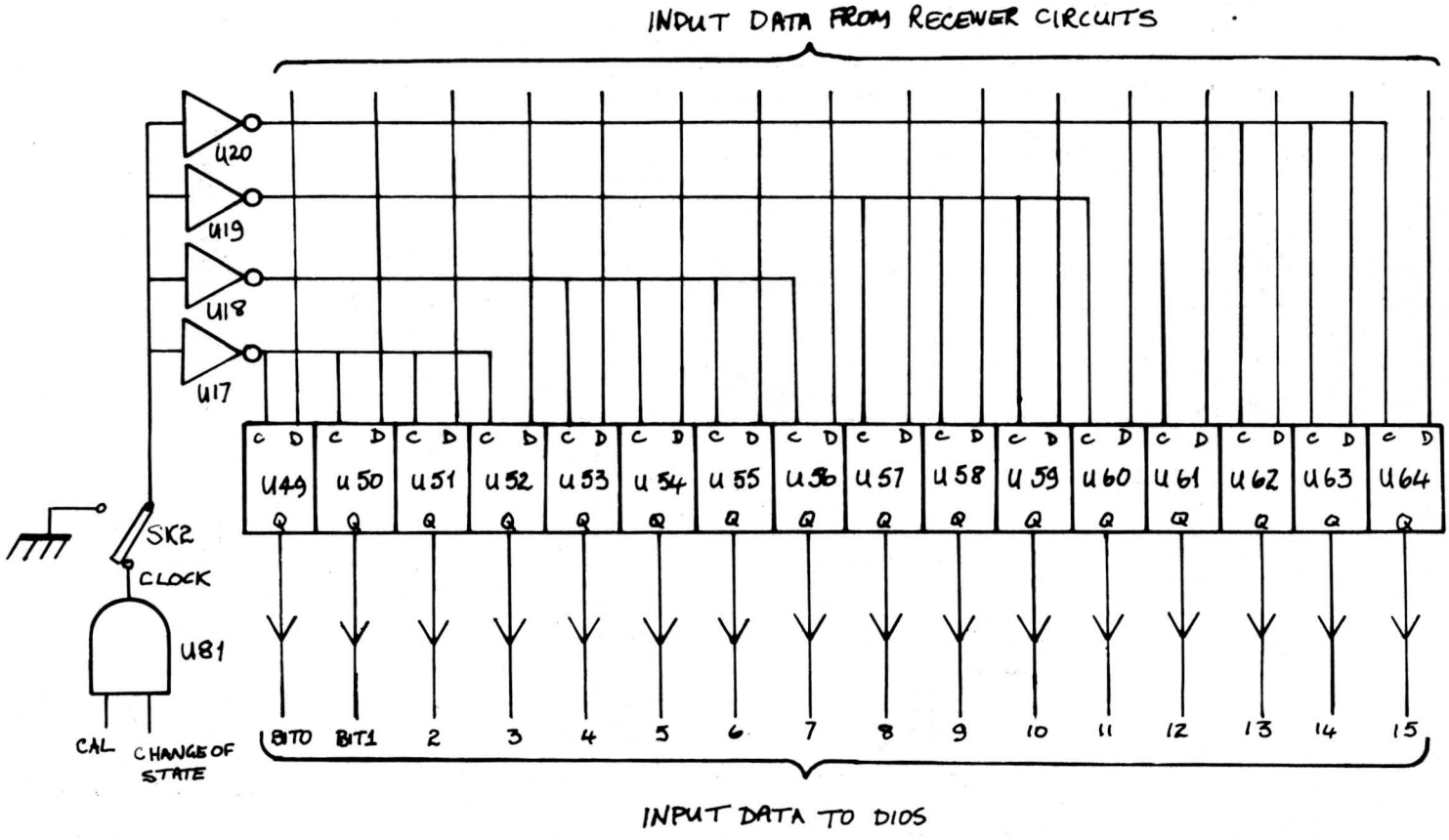


FIGURE 5.10 INPUT BUFFER

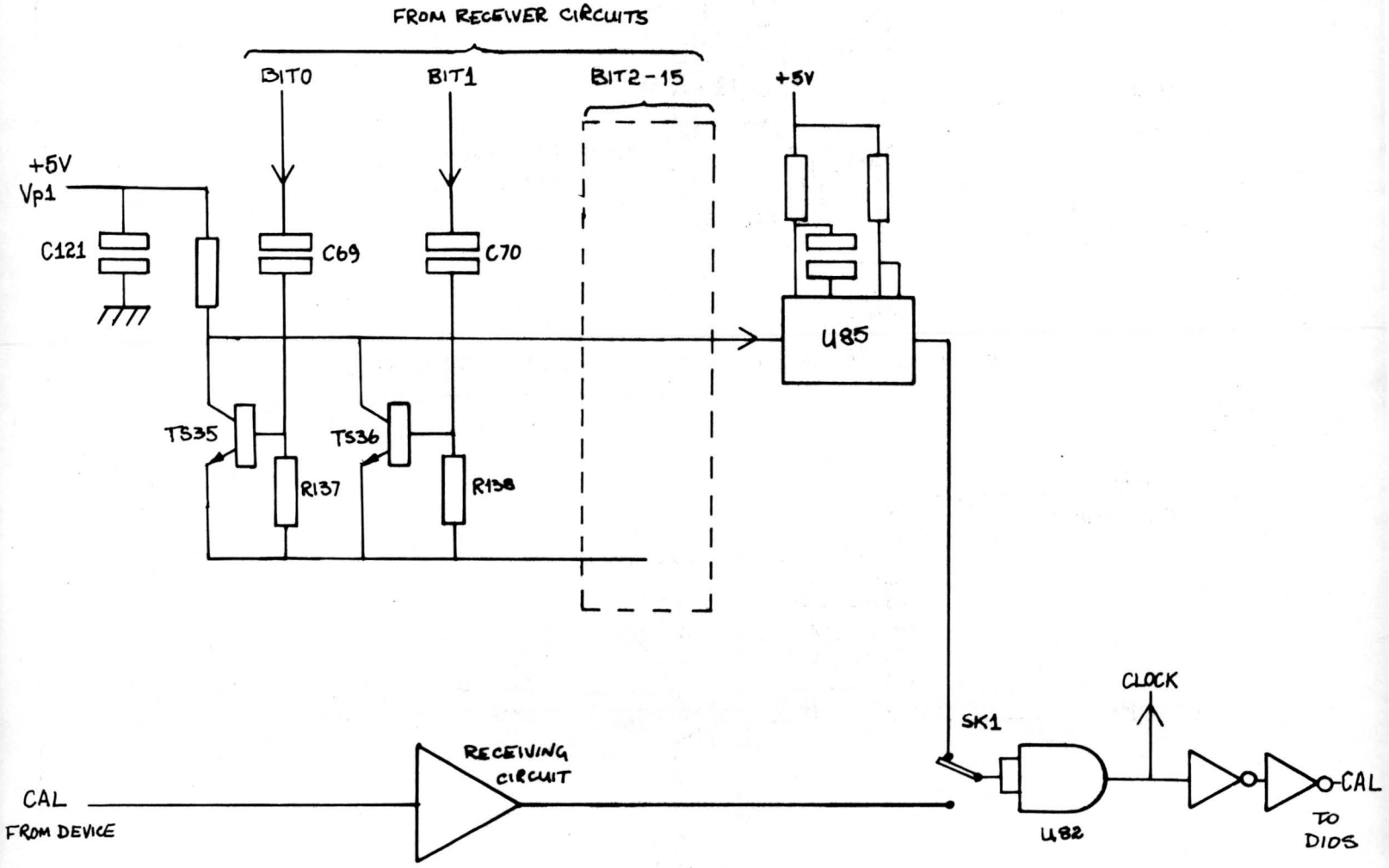


FIGURE 5.11 CHANGE OF STATE DETECTION CIRCUIT

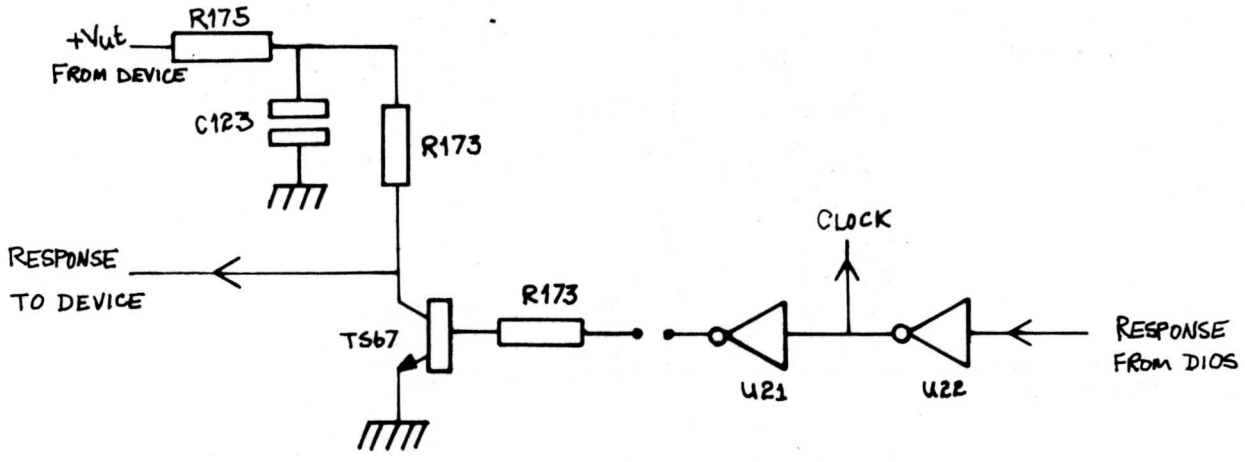


FIGURE 5.12 TRANSMITTER CIRCUIT

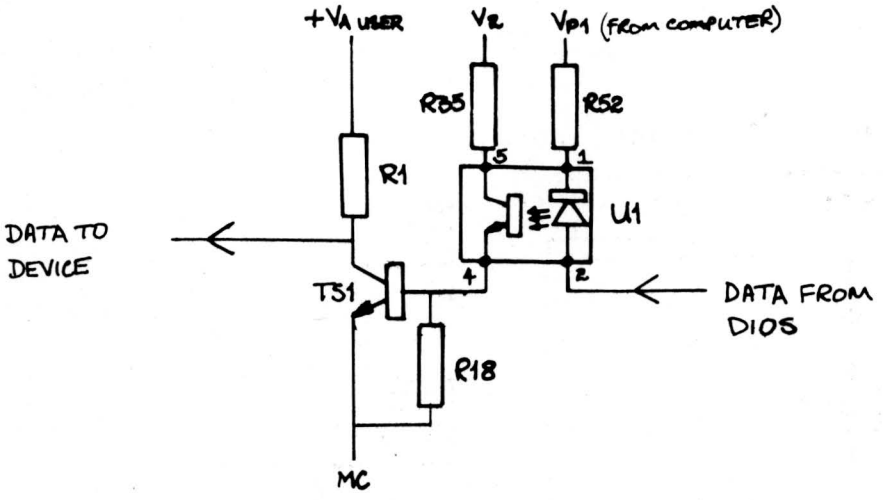


Fig. 5.13 TRANSMITTER AND ISOLATOR CIRCUIT

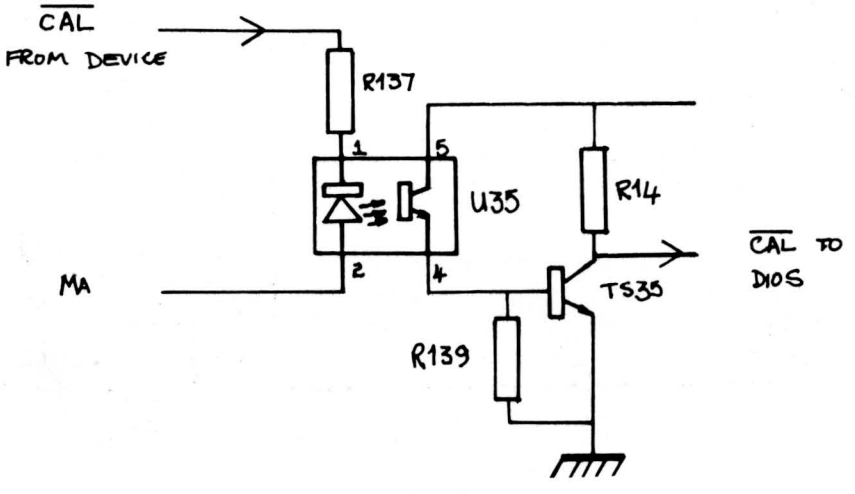


Fig. 5.14 RECEIVER AND ISOLATOR CIRCUIT

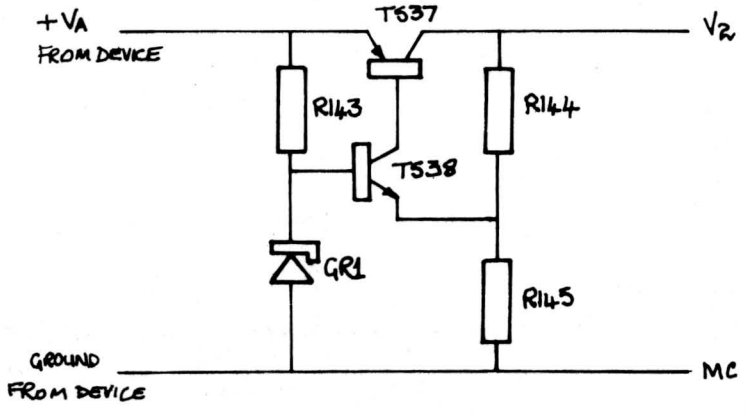


Fig. 5.15 VOLTAGE REGULATOR

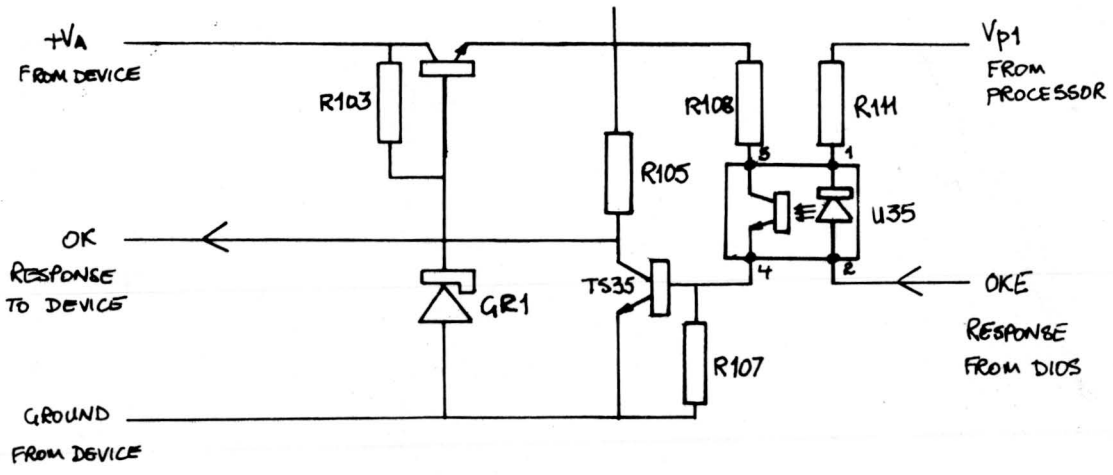


Fig. 5.16 VOLTAGE REGULATOR, TRANSMITTER AND ISOLATOR CIRCUIT

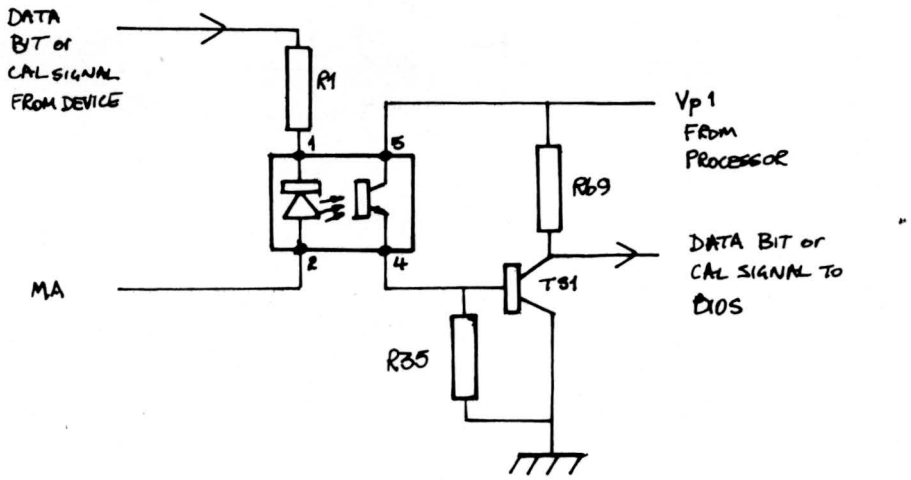


Fig. 5.17RECEIVER AND ISOLATOR CIRCUIT

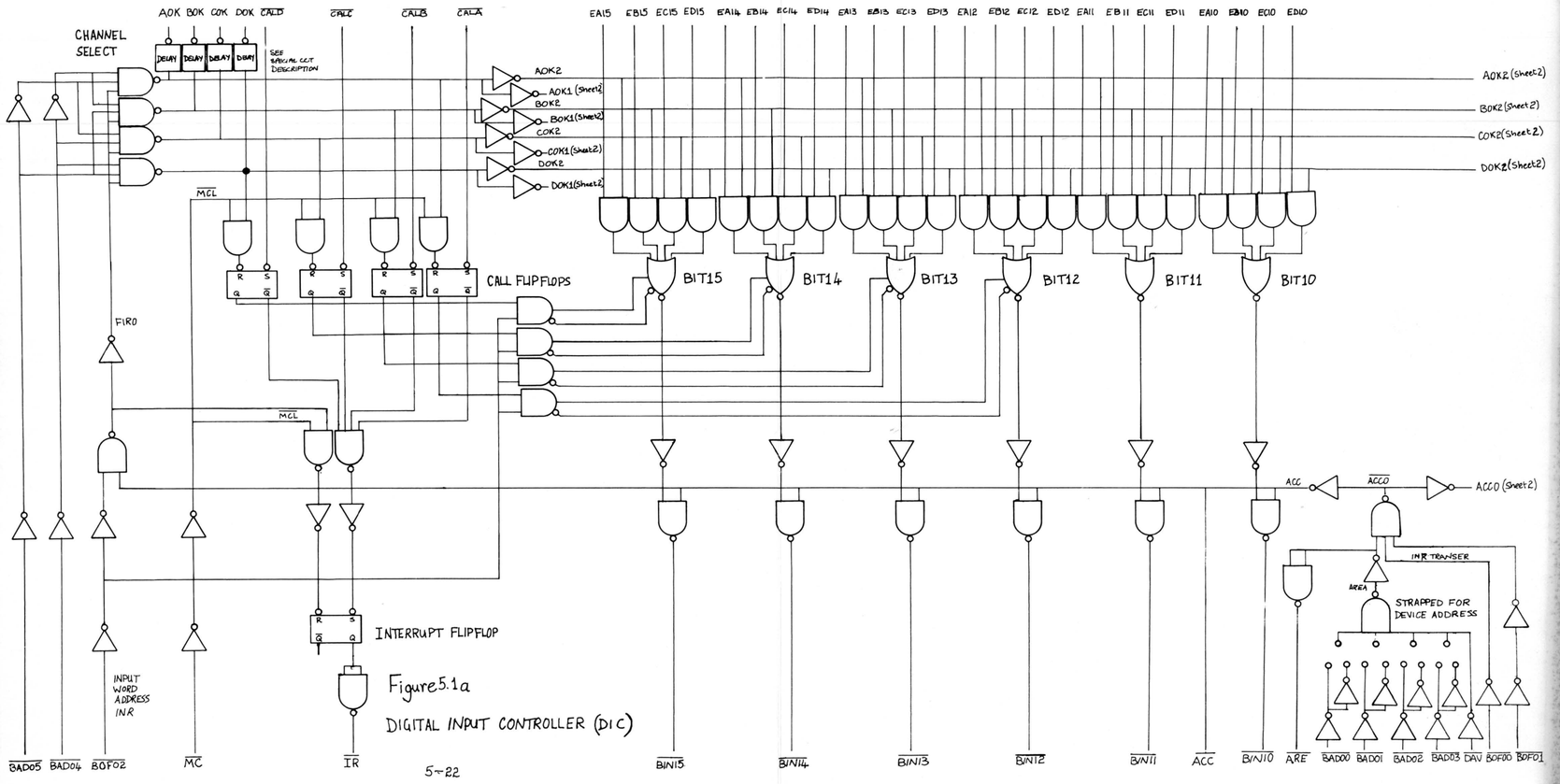


Figure 5.1a

DIGITAL INPUT CONTROLLER (DIC)

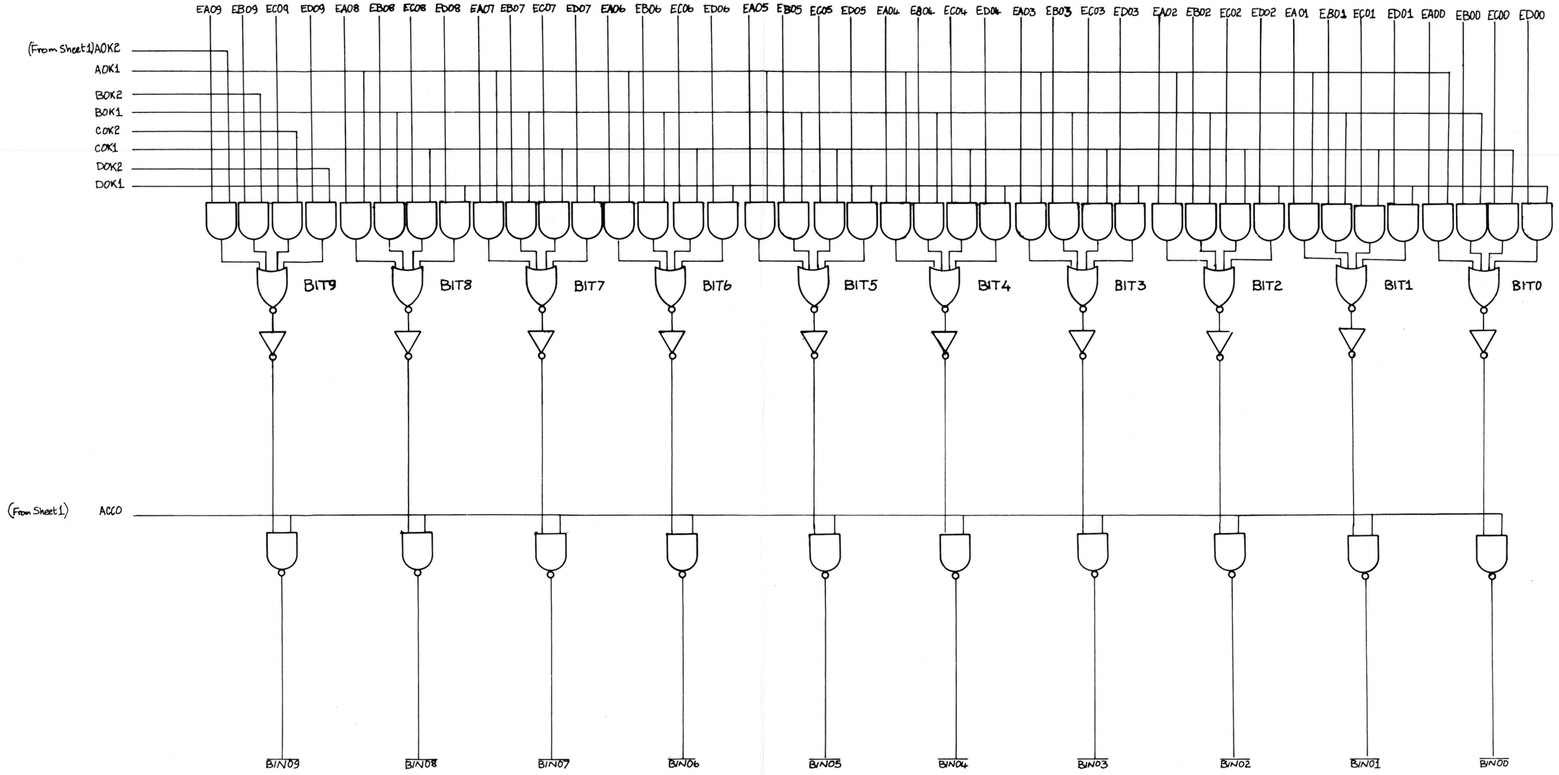


Figure 5.1b DIGITAL INPUT CONTROLLER

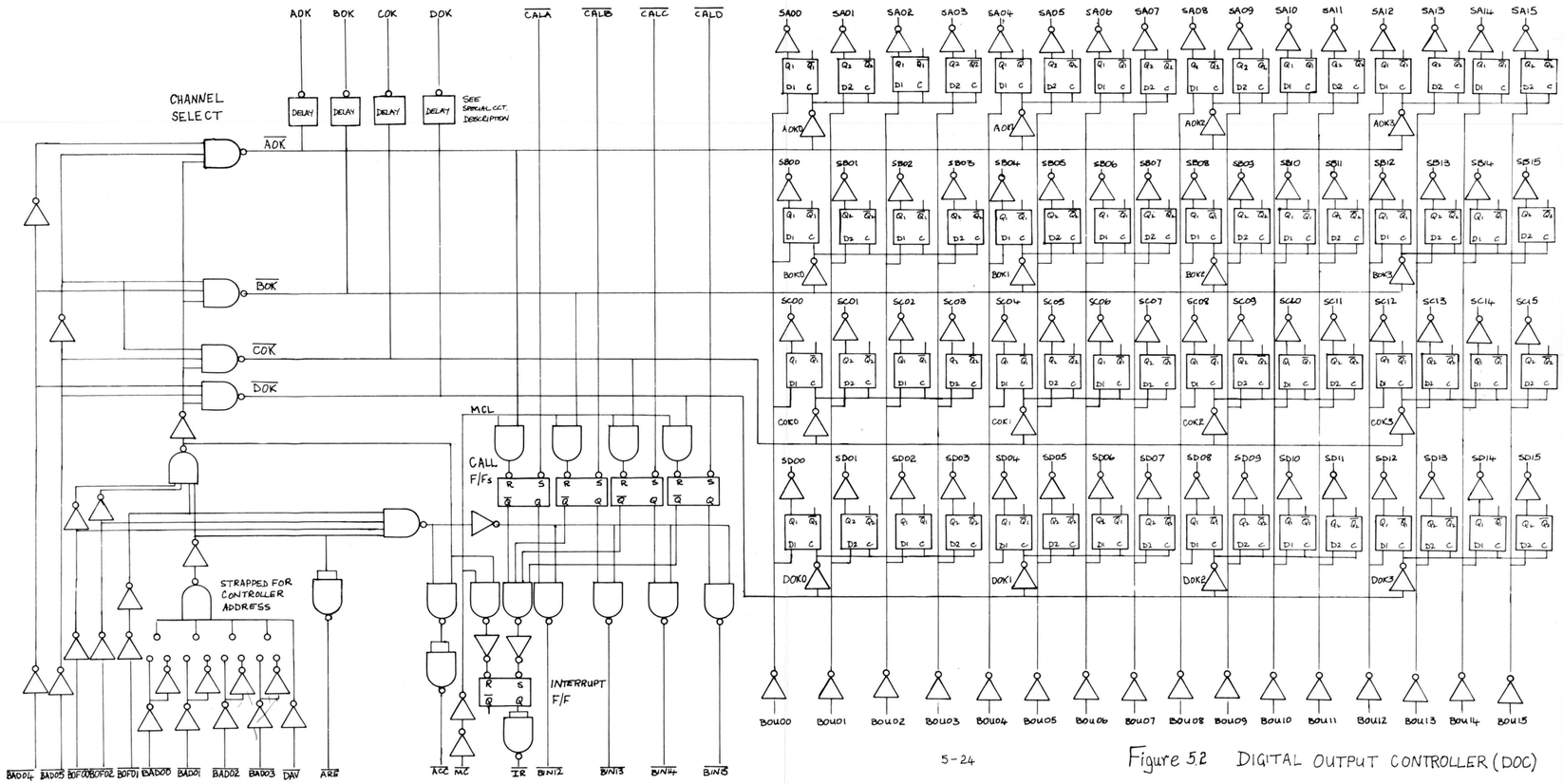


Figure 5.2 DIGITAL OUTPUT CONTROLLER (DOC)

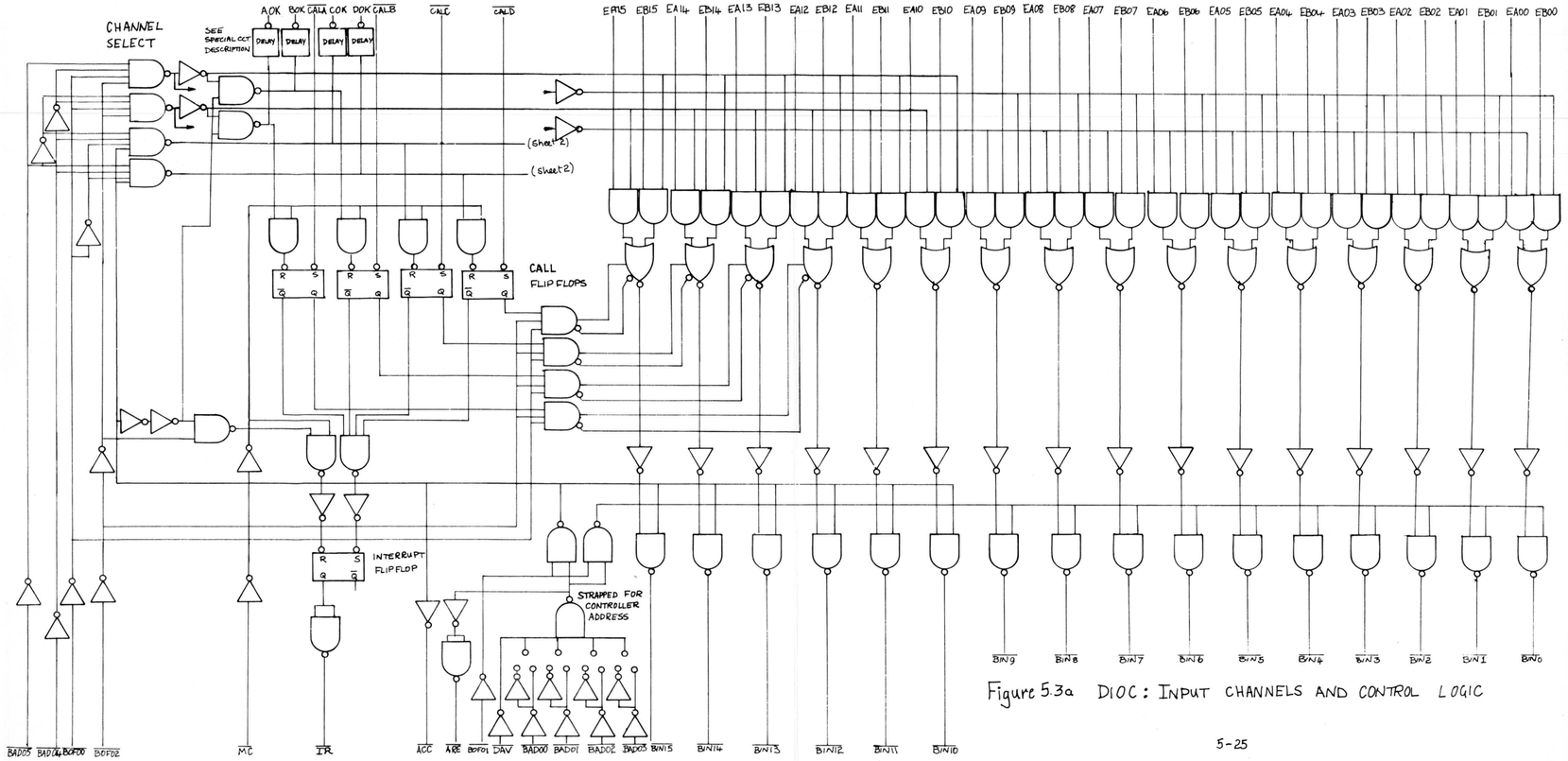


Figure 5.3a DIOC: INPUT CHANNELS AND CONTROL LOGIC

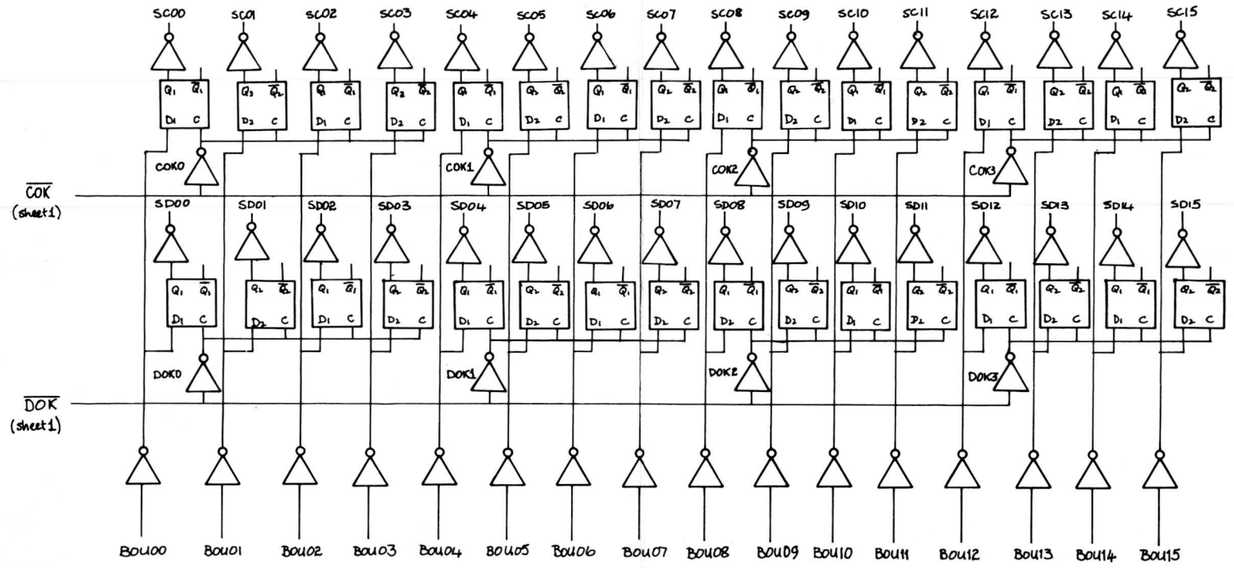


Figure 5.3b DIOC: OUTPUT CHANNELS

SECTION VI

LINE PRINTER CONTROL UNIT

BRIEF DESCRIPTION

The Line Printer Control Unit provides the interface and control logic to transfer information from the central processor to the Line Printer. The control unit may be used with either the programmed channel or the multiplex channel of the central processor; the mode is selected prior to installation and is not program changeable. The control unit is contained on one card and may be used with either of the following line printers:

Data Products model 2310

Data Products model 2410 or 2420

Data Products model 2440

Figure 6.2 is a Block Diagram of the control unit.

6.1 PRINT COMMANDS

The format of the data sent is seven bit (Output Bus lines BOU15-09) plus one Paper Instruction (PI) indicator on BOU08. If the PI bit is zero the other seven bits are loaded into the Line Printer's buffer and eventually printed with the exception of the following three characters which are decoded by the line printer as commands:

MNEMONIC	MEANING	CODE
PF	Paper Feed - advances the paper one line and causes a CR	BOU 15 14 13 12 11 10 9 8 0 1 0 1 0 0 0 0
FF	Form Feed - advances the paper to the top of the next sheet of paper and gives a CR	0 0 1 1 0 0 0 0
CR	Carriage Return - sets the printer at the left-most print position	1 0 1 1 0 0 0 0

If the PI bit is one then the other seven bits are considered to be a vertical format character. This character indicates to the Line Printer that the paper must be moved either to a position indicated by the character itself or by the Line Printer's control paper tape. If bit 11 is zero the line printer advances

the paper until the next hole is encountered in the control paper tape channel specified by bits 15 - 13.

BOU	15	14	13	12	11	10	9	8
Paper tape channel No.	0	0	X	1	1			

If bit 11 is one the line printer advances the paper the number of lines specified by bits 15 -12.

BOU	15	14	13	12	11	10	9	8
Number of lines Skipped	1	X	1	1				

6.2 ADDRESSING

The address of the control unit may be selected using straps which connect the address decode gate in the CU to the computer BAD lines BAD00-05. The address part of instructions is checked when a validity signal DAV/ is received from the computer. If the address is accepted the signal ARE/ is returned to the computer and command decoding is enabled.

6.3 COMMAND DECODING

The setting of the bits on BOF lines 00-02 determine the function of instructions sent to the controller. These bits are decoded by the 1 out of 10 decoder module 9301 the signal AREA/ enables the decoding once the CU's address has been recognised. The commands recognised by the control unit are:

BOF 00	01	02	COMMAND	OPERATIONAL STATE REQUIRED	FUNCTION
1	1	0	Test Status	Any	To determine the status of the control unit
0	1	1	CIO Start	Inactive	To initiate the transfer of a block of information
0	1	0	CIO Stop	Any	Halt CPU/CU transfer
0	0	X	OTR Command	Exchange	To transfer one 8-bit character
1	1	1	SST Send Status	Wait Status	Transfer line printers status to CPU

X the setting of this bit is not important.

The signal ACC/ is returned to the CPU when the command is recognised.

6.4 OPERATIONAL STATES

The control unit functions in four operational states (INACTIVE, EXCHANGE, EXECUTE and WAIT STATUS) and switches between them as a result of signals received from either the CPU or the device. Figure 6.3 shows the interworking of the operational states. The code shown on thediagram next to the name of each state is the true output from the Operational State Register (flip flops F0 and F1) which determine the state of the controller.

INACTIVE This is an idle condition for the CU to which it returns after completing the transfer of a block of information to the printer (see WAIT STATUS). The command CIO START is required, if the CU is in the INACTIVE state, to initiate a data transfer. Provided the line printer is OPERABLE the command toggles both the F0 and F1 flip flops putting the control unit into EXCHANGE state, otherwise the Halt flip flop is set and the control unit is switched into the WAIT STATUS state. The CIO START command can only be received while the CU is in the INACTIVE state.

EXCHANGE The EXCHANGE state is used to load one eight bit character from the CPU output bus into the Output Buffer in the CU and to prepare the CU to transfer this character to the line printer. As soon as the CU switches to the EXCHANGE state an interrupt (PIL/) or Break Request (BR/) if the CU is connected to the multiplex channel, is sent to the processor to request a data transfer. The CPU responds to the request with an OTR Output command and places the data for transfer on BOU lines 08-15. The OTR command (ACOTR/) clocks the data on the BOU lines into the CUs Output Buffer, sets the Strobe flip flop and puts the CU into the EXECUTE state.

EXECUTE This state is used to transfer the data from the CU to the Line Printer and to receive requests from the printer for further data transfers. When the CU switches to the EXECUTE state the signal EXT/goes low and with FSTROBE/ produces the STROBE signal to transfer the data from the Output Buffer to the Line Printer. The Line Printer stores each printable character transferred and sends demands for new characters until either its buffer is full or until a print command is received from the control unit. In both cases the line printer prints the contents of its buffer and in the latter case also obeys the print command afterwards. The DEMAND signal received

from the printer resets the FSTROBE flip flop and sets the Operational State Register back into EXCHANGE state; this causes a new character request to be sent to the CPU.

WAIT STATUS The CU uses WAIT STATUS to transfer a status word to the CPU. It is normally entered from the EXCHANGE state after the CPU has either sent the last character with an End of Range (EOR) signal, for multiplex channel transfers, or a CIO STOP command, for program channel transfers. WAIT STATUS is also entered if the Line Printer becomes inoperable. All of these conditions cause the HALT flipflop to be set which sends a Status Request Interrupt (PIL/) to the CPU. The control unit must then wait for a Send Status (SST/) command from the processor to place the device status on the Input Bus line BIN15. BIN15 is set if the Line Printer is not operable: BIN lines 14-08 have no significance. The command SST sets the control unit into the INACTIVE state and resets both the HALT and STROBE flip flops.

6.5 RESETTING

A Master Clear signal (MC/) may be sent from the processor to reset both the Halt and Strobe flip flops and to set the Operational State register into the INACTIVE state.

6.6 INTERRUPTS

If the control unit is connected to the multiplex channel a DEMAND signal received from the Line Printer will cause a Break Request signal (BS/). If the program channel is used the signal is strapped across to give a program interrupt (PIL/) (see EXECUTE). Regardless of whether the program channel of multiplex channel is used a program interrupt (PIL/) is used as a status request whenever the Halt flip flop is set (see WAIT STATUS). Setting the Halt flip flop prevents demands from the line printer from causing are interrupt or break request.

6.7 TEST STATUS

The Test Status command may be sent to determine if the control unit is busy. It is always accepted and BIN15 is set to a one if the CU is not in the INACTIVE state.

6.8 CU TO LINE PRINTER CONNECTIONS

Connections between the control unit and the line printer are made using twisted pair wires between ELCO connectors. One of the wires is connected to ground both at the CU and at the line printer and the other is connected to the appropriate signal.

6.9 TIMING

Figure 6.4 shows the sequence of operations required to initiate and continue a data transfer from the CPU to the Line Printer. Figure 6.5 shows the status request and sending sequence.

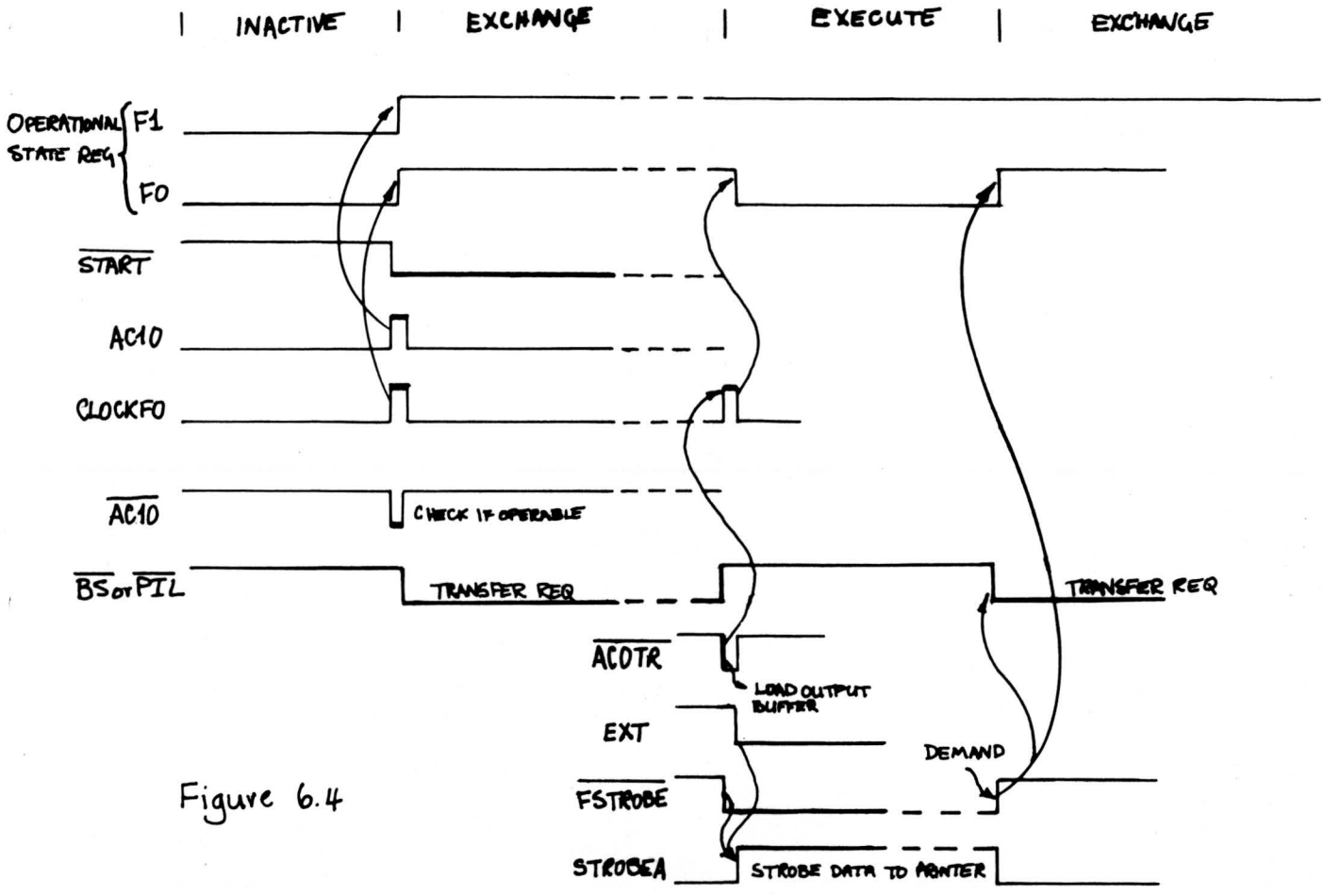


Figure 6.4

The EXCHANGE/EXECUTE cycle is repeated until all the data has been transferred. If the data transfer is controlled by the program channel a HALT command will normally be programmed at the end of the transfer. An EOR (End of Range) signal is used in place of the HALT instruction when the multiplex channel is used for the transfer.

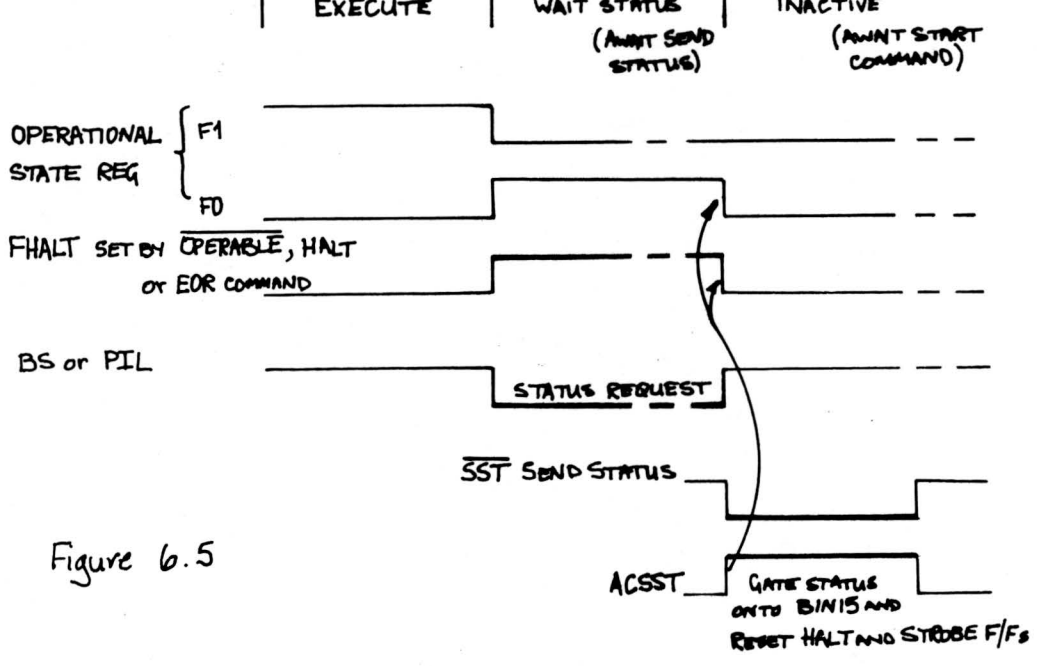


Figure 6.5

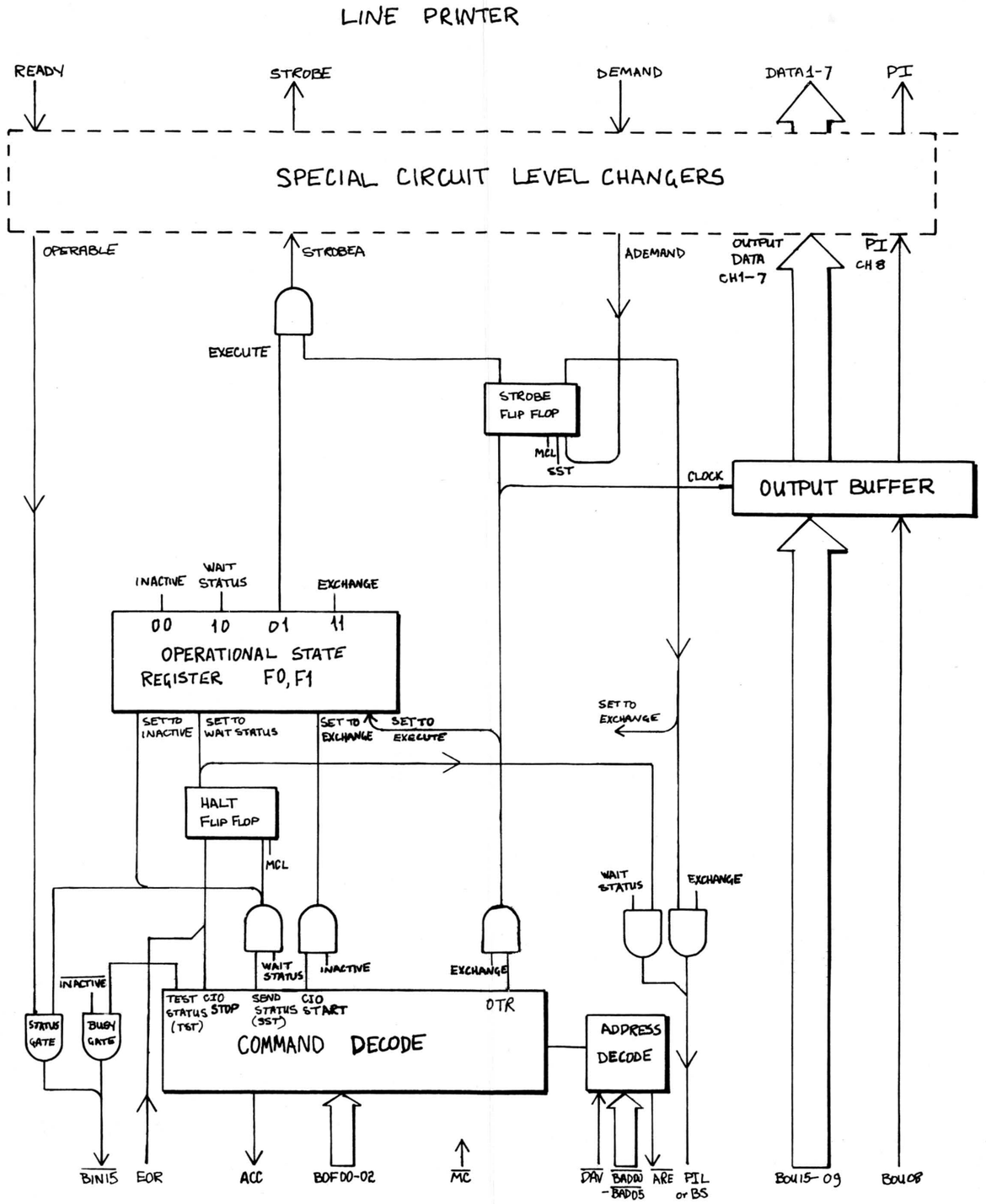
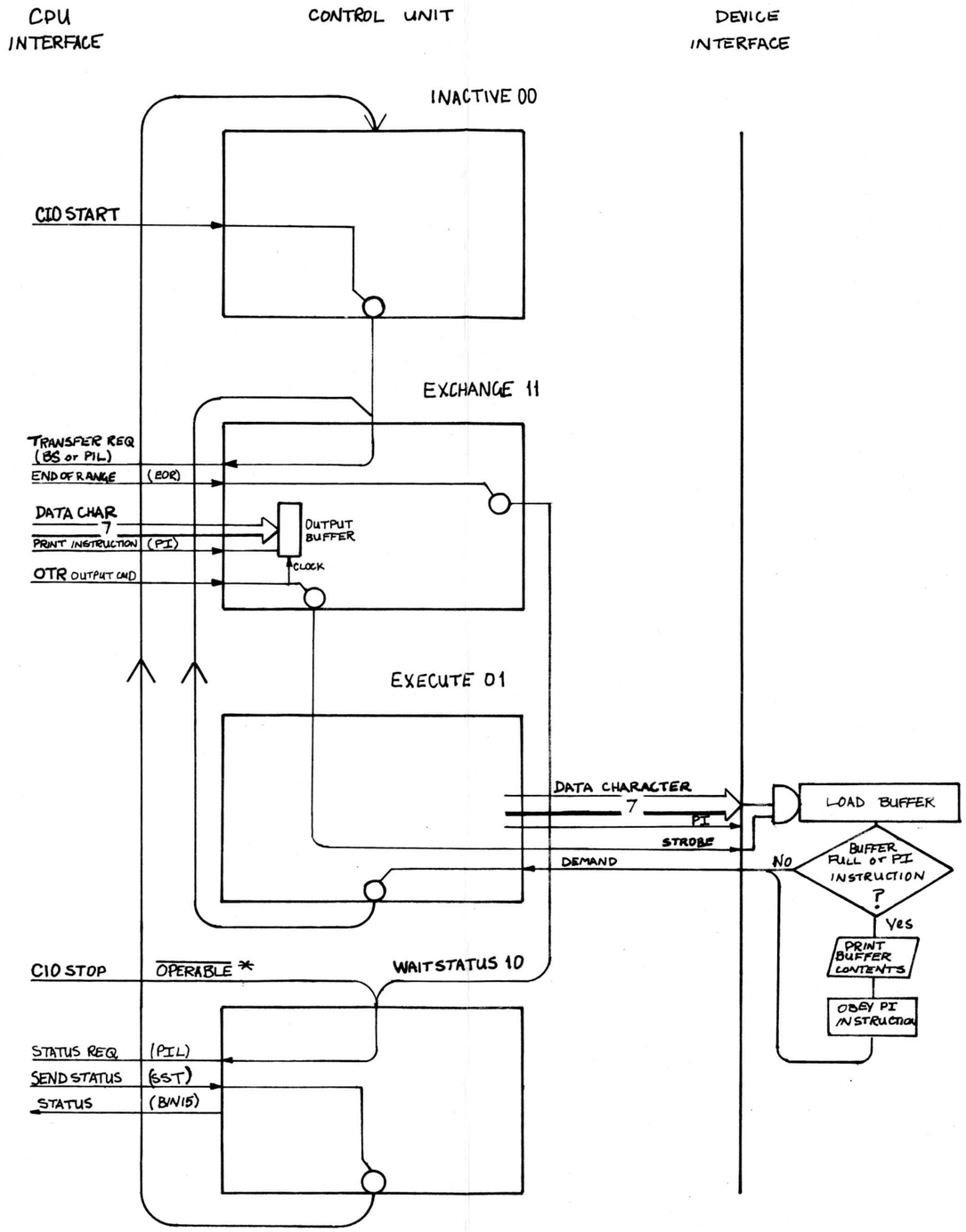


Figure 6.2 BLOCK DIAGRAM



* THESE SIGNALS MAY BE RECEIVED WHILE THE CONTROLLER IS IN ANY OF THE OTHER THREE OPERATIONAL STATES.

Figure 6.3 OPERATIONAL STATES

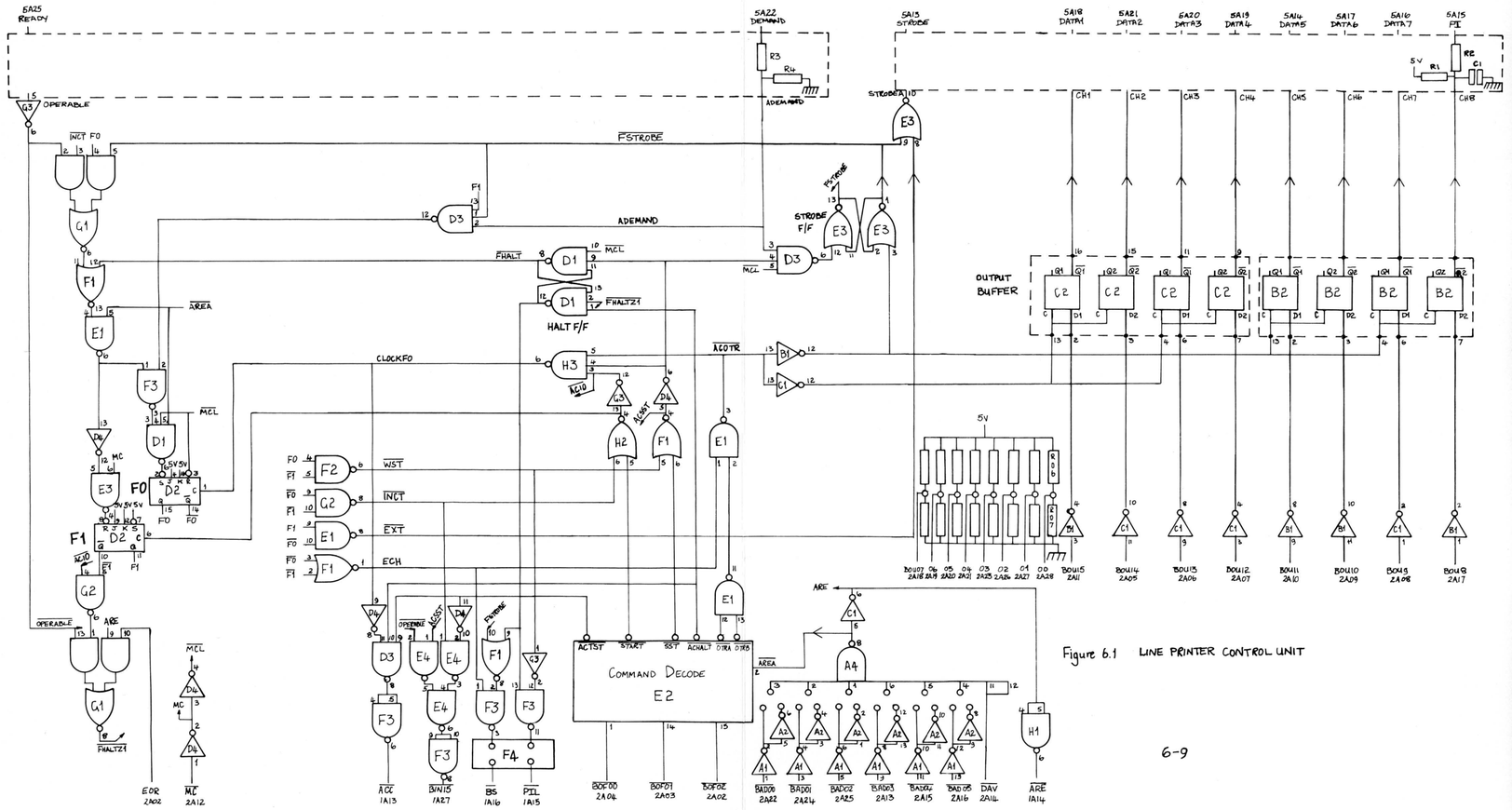


Figure 6.1 LINE PRINTER CONTROL UNIT